AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (Cancelled)

2. (Cancelled)

3. (Cancelled)

4. (Cancelled)

5. (Cancelled)

6. (Currently Amended): A latch circuit, comprising:

a first latch portion including a first clock transistor; and

a second latch portion including a second clock transistor[[;]],

wherein the first and second clock transistors form a transistor clock pair and each of the clock transistors receiving complementary clock inputs to define a 'hold period/follow period' ratio for the transistor clock pair, the first clock transistor having a different emitter area to that of ~~has a different property~~

~~or characteristic to~~ the second clock transistor, ~~such that a ratio of a hold period to a follow period of the transistor clock pair is greater than 1.~~

wherein the emitter area of the first clock transistor is greater than that of the second clock transistor such that the 'hold period/follow period' ratio of the transistor clock pair is greater than 1.

7. (Previously Presented) The latch circuit according to claim 6, wherein the different property or characteristic comprises a difference in emitter area.

8. (Previously Presented) The latch circuit according to claim 7, wherein the emitter area of the first clock transistor is greater than that of the second clock transistor.

9. (Previously Presented) The latch circuit according to claim 8, wherein the emitter area of the first clock transistor is double that of the second clock transistor.

10. (Previously Presented) A prescaler circuit including a first and second latch circuit according to claim 6.

11. (Previously Presented) A prescaler circuit including a first and second latch circuit according to claim 7.

12 (Previously Presented) A prescaler circuit including a first and second latch circuit according to claim 8.

13. (Previously Presented) A prescaler circuit including a first and second latch circuit according to claim 9.

14. (New) The latch circuit according to claim 6, wherein the first latch portion is a master latch, and the second latch portion is a slave latch.